REMARKS

Claims 1, 15, 19, and 23 have been amended, and claims 1-24 are pending in the present application. The claim amendments are supported by the specification and drawings as originally filed, with no new matter being added. Accordingly, favorable reconsideration of the pending claims is respectfully requested.

1. Specification

The specification was objected to as failing to provide proper antecedent basis for the claimed subject matter for the reasons set forth on page 2 of the Office Action. Applicants respectfully traverse.

While Applicants disagree with the objection to the specification, Applicants have further amended the claimed subject matter in response to the objection. Thus, Applicants request that the objection to the specification be withdrawn.

2. Rejections Under 35 U.S.C. § 112

Claims 1-24 have been rejected under 35 U.S.C. §112, first paragraph, as containing subject matter that was not described in the specification in such a way as to convey to one skilled in the art that the inventors, at the time the application was filed, had possession of the claimed invention. Applicants respectfully traverse.

While Applicants disagree with this rejection of the claims, Applicants have further amended independent claims 1, 15, 19, and 23 along the lines suggested by the Examiner on page 3 of the Office Action. Thus, Applicants request that the rejection of claims 1-24 under 35 U.S.C. § 112, first paragraph, be withdrawn.

3. Rejections Under 35 U.S.C. § 102

Claims 1-2, 6, 9, 12-13, 15, 17, 19-20, and 22-24 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,343,354 to Lee et al. (hereinafter "*Lee*") for the reasons set forth on page 3 of the Office Action. Applicants respectfully traverse.

Claim 1 has been amended to recite "forming a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide extends below the upper surface of said semiconductor substrate." Similar limitations are also now recited in independent claims 15, 19, and 23. Support for these limitations can be found in the application as filed on page 8, paragraph [023], and in Figures 6 and 7 of the drawings.

Lee teaches that a gate insulating layer 1 such as an oxide layer is formed on the upper surface of the semiconductor substrate 100 (col. 5, lines 54-57). As shown in Figure 4B of *Lee*, the gate insulating layer 1 is above the upper surface of substrate 100. Thus, there is no teaching or suggestion in *Lee* that the gate oxide extends below the upper surface of the semiconductor substrate as recited in present claims 1, 15, 19, and 23.

Hence, claims 1, 15, 19 and 23 are not anticipated by *Lee*. Claims 2, 6, 9, and 12-13 depend from claim 1, claim 17 depends from claim 15, and claims 20 and 22 depend from claim 19. Thus, these dependent claims each include the limitations of the respective independent claim, and are also not anticipated by *Lee* for at least the same reasons as stated above.

Independent claim 24 recites that the "cell plate has an upper surface that extends into said container cell." Such a feature is not taught or suggested in *Lee*. Rather, *Lee* discloses (Fig. 4E) that the plate electrode PE is formed over dielectric 20 such that the upper surface of the plate electrode is above the trench (cell). Thus, claim 24 is not anticipated by *Lee*.

Accordingly, Applicants respectfully request that the rejection of claims 1-2, 6, 9, 12-13, 15, 17, 19-20, and 22-24 under 35 U.S.C. § 102(b) be withdrawn.

4. Rejections Under 35 U.S.C. § 103

Claims 3, 8, and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 2) for the reasons set forth on page 4 of the Office Action. In addition, claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 3) for the reasons set forth on page 4 of the Office Action. Further, claims 10 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of *Wolf* (Vol. 1) for the reasons set forth on page 4 of the Office Action. Applicants respectfully traverse.

Claims 3, 7, 8, 10, and 11 depend from claim 1, and claim 18 depends from claim 15. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that "the gate oxide extends below the upper surface of said semiconductor substrate." As discussed previously, this limitation is not taught or suggested in *Lee*. In addition, such a feature is also not taught or suggested in *Wolf* (Vol. 1-3). Hence, claims 3, 7, 8, 10, 11, and 18 would not have been obvious over *Lee* in view of *Wolf* (Vol. 1-3).

Applicants therefore respectfully request that the rejection of claims 3, 7, 8, 10, 11, and 18 under 35 U.S.C. § 103(a) be withdrawn.

Claims 4, 5, and 16 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* in view of U.S. Patent No. 6,114,216 to Yieh et al. (hereinafter "*Yieh*") for the reasons set forth on page 5 of the Office Action. Applicants respectfully traverse.

Claims 4 and 5 depend from claim 1, and claim 16 depends from claim 15. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that "the gate oxide extends below the upper surface of said semiconductor substrate." As discussed previously, this limitation is not taught or suggested in *Lee*. In addition, such a feature is also not taught or suggested in *Yieh*. Hence, claims 4, 5, and 16 would not have been obvious over *Lee* in view of *Yieh*.

Applicants therefore respectfully request that the rejection of claims 4, 5, and 16 under 35 U.S.C. § 103(a) be withdrawn.

Claims 14 and 21 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over *Lee* for the reasons set forth on page 5 of the Office Action. Applicants respectfully traverse.

Claim 14 depends from claim 1, and claim 21 depends from claim 19. Thus, these dependent claims each include the limitations of the respective independent claim, including the recitation that "the gate oxide extends below the upper surface of said semiconductor substrate." As discussed previously, this limitation is not taught or suggested in *Lee*. Hence, claims 14 and 21 would not have been obvious over *Lee* for at least the same reasons as discussed above for claims 1 and 19.

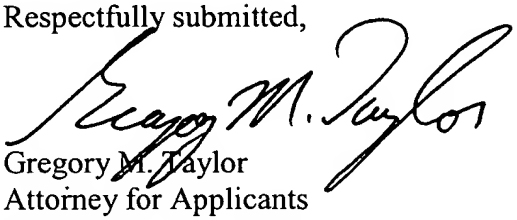
Applicants therefore respectfully request that the rejection of claims 14 and 21 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing, Applicants respectfully request favorable reconsideration and allowance of the pending claims. In the event the Examiner finds any impediment to the prompt allowance of this application that could be clarified by a telephone interview, the Examiner is respectfully requested to contact the undersigned attorney.

Dated this 14th day of February 2003.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW THE CHANGES MADE

IN THE CLAIMS:

Claims 1, 15, 19, and 23 have been amended as follows:

1. (Twice Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming an isolation film within said trench[, said isolation film having an upper surface];

forming a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide [has an upper surface that is substantially coplanar with the upper surface of said isolation film] extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks.

15. (Twice Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming a conformal isolation film within said trench[, said isolation film having an upper surface];

[forming] growing a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide [has an upper surface that is substantially coplanar with the upper surface of said isolation film] extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film have an interface that extends below said edge into said semiconductor substrate.

19. (Twice Amended) A process of forming a container cell, comprising:

forming a trench in a semiconductor substrate by spinning on a photoresist, masking, exposing and patterning said photoresist to create a photoresist mask, and anisotropically etching through said photoresist mask, said semiconductor substrate having an upper surface;

forming a conformal isolation film within said trench by forming an oxide film by deposition[, said isolation film having an upper surface];

[forming] growing a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide [has an upper surface that is substantially coplanar with the upper surface of said isolation film] extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate and having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench; and

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks, wherein said semiconductor substrate and said isolation film form an interface that extends below said container cell into said semiconductor substrate.

23. (Once Amended) A process of forming a capacitor, comprising:

forming a trench in a semiconductor substrate, said semiconductor substrate having an upper surface;

forming an isolation film within said trench[, said isolation film having an upper surface];

forming a gate oxide on the upper surface of said semiconductor substrate such that the gate oxide [has an upper surface that is substantially coplanar with the upper surface of said isolation film] extends below the upper surface of said semiconductor substrate;

forming a first gate stack upon said semiconductor substrate, said first gate stack having an edge aligned with and adjacent to an edge of said trench;

forming a second gate stack upon said isolation film within said trench;

etching a container cell into said isolation film within said trench, said container cell being situated substantially between said first and second gate stacks and having an edge defined by said semiconductor substrate and said isolation film, said edge of said container cell substantially extending to and terminating at each of said first and second gate stacks;

forming a storage node within said container cell;

forming a cell dielectric upon said storage node; and

forming a cell plate upon said first gate stack, upon said cell dielectric, and upon said second gate stack.